REMARKS

Claims 1-20 are pending in the present application. Reconsideration and allowance of pending claims 1-20 in view of the following remarks are requested.

A. Rejection of Claims 1-5, 8-12, and 15-19 under 35 USC §102(b)

The Examiner has rejected claims 1-5, 8-12, and 15-19 under 35 USC §102(b) as being anticipated by U.S. patent number 5,886,925 to Compardo et al. ("Compardo"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 1, 8, and 15, is patentably distinguishable over Campardo.

The present invention, as defined by independent claims 1 and 15, includes, among other things, a decouple circuit being connected to a first transistor, where the decouple circuit includes a second transistor having a gate width greater than a gate width of the first transistor, where the decouple circuit has a decouple coefficient (N) greater than 1, and where a drain of the second transistor is connected at a second node to a reference voltage through a bias resistor. As disclosed in the present application, the present invention provides a sensing circuit including first and second transistors and a decouple circuit, which includes a third transistor having a drain that is coupled to ground through a resistive load. As disclosed in the present application, a drain of the second transistor is coupled to a first node, a gate of the first transistor is coupled to a gate of the third transistor, and the gate of the third transistor is N times wider than the gate of the first transistor.

As a result of the above circuit arrangement, a sense amp input voltage generated at the drain of third transistor, which corresponds to a current drawn by a target memory cell coupled to a source of the second transistor, is decoupled from a voltage generated at the source of the second transistor during activation of the target memory cell. As a result, the present invention's sensing circuit advantageously achieves a significantly improved sensing margin for detecting the state of the target memory cell during read operations, particularly for reduced voltage requirements in certain applications. By significantly improving the sensing margin for detecting the state of the target memory cell, the present invention's sensing circuit advantageously achieves efficient and accurate memory cell sensing. Additionally, the present invention advantageously achieves the above advantages in high density memory devices, where each memory cell is capable of storing multiple charge levels.

In contrast to the present invention as defined by independent claims 1 and 15, Compardo does not teach, disclose, or suggest a decouple circuit being connected to a first transistor, where the decouple circuit includes a second transistor having a gate width greater than a gate width of the first transistor, where the decouple circuit has a decouple coefficient (N) greater than 1, and where a drain of the second transistor is connected at a second node to a reference voltage through a bias resistor. Compardo is directed to a read circuit for nonvolatile memory cells with an equalizing structure. Compardo specifically discloses read circuit 1 including current/voltage converter 9, which includes reference load transistor 13 coupled to array load transistor 12 in a current mirror configuration. See, for example, column 1, lines 66-67, column 2, lines 1-20, and Figure 1 of Compardo. In Compardo, array load transistor 12 has a width/length ratio equal to N*K, while reference load transistor 13 has a width/length ratio equal to K. However, Compardo does not teach, disclose, or suggest any relationship between the length of array load transistor 12 and the length of reference load transistor 13 or any relationship between the width of array load transistor 12 and the width of reference load transistor 13. Thus, Compardo fails to teach, disclose, or suggest that the gate width of reference load transistor 13 is greater than the gate width of array load transistor 12.

Also, in Compardo, circuit 10 couples the drain of reference load transistor 13 to reference cell 7, which is connected to ground. See, for example, Figure 1 of Compardo. Thus, in Compardo, the drain of reference load transistor 13 is coupled to ground via the series combination of circuit 10 and reference cell 7. However, Compardo fails to teach, disclose, or suggest a drain of the second transistor being connected at a second node to a reference voltage through a bias resistor, as specified in independent claims 1 and 15. Furthermore, Compardo fails to teach, disclose, or suggest a decouple circuit having a decouple coefficient (N) greater than 1. Although Compardo discloses multiplication constant N related to the current mirror formed by array load transistor 12 and reference load transistor 13, Compardo fails to even mention a decouple circuit or a decouple coefficient.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claims 1 and 15, is not suggested, disclosed, or taught by Compardo. As such, the present invention, as defined by independent claims 1 and 15, is patentably distinguishable over Compardo. Thus claims 2-7 depending from independent claim 1 and claims 16-20 depending from independent claim 15 are, *a fortiori*, also patentably distinguishable over Compardo for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The present invention, as defined by independent claim 8, includes, among other things, a decouple circuit in a multi-level charge memory device being connected to a first transistor, where the decouple circuit includes a second transistor having a gate width greater than a gate width of the first transistor, where the decouple circuit has a decouple coefficient (N) greater than 1, and where a drain of the second transistor is connected at a second node to a reference voltage through a bias resistor. Independent claim 8 recites similar limitations as independent claim 1 discussed above. Additionally, independent claim 8 recites a multi-level charge memory device, which is not taught, disclosed, or even suggest by Compardo. Thus, for at least the reasons discussed above, independent claim 8 is also patentably distinguishable over Compardo. Thus, claims 9-14 depending from independent claim 8 are, *a fortiori*, also patentably distinguishable over Compardo for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1, 8, and 15 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-20 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-20 pending in the present application is respectfully requested.

Respectfully Submitted,
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